IN THE CLAIMS:

Please amend the claims as follows:

1.   (Original)   A Viterbi decoder for decoding a convolutional code on the basis of a Radix-2^x trellis with 2^z states, where x and z are integers greater than 1, comprising:

a first calculation unit for calculating 2^x branch metrics as m-bit words using periodically successive multibit words in an input sequence for each trellis state;

a second calculation unit having parallel cascades of processor elements for adding the 2^x branch matrics calculated by the first calculation unit to accumulated 2^x path metrics from 2^x predecessor trellis states and a selection device for selecting a subset of the 2^x path metrics for use as accumulated 2^x path metrics in an addition process in a subsequent clock period, wherein the number of processor elements in each of the cascades is less than the number m of the m-bit words; and

a third calculation unit for storage of information obtained from the second calculation unit relating to the identity of the selected path metrics.

2.   (Original)   The Viterbi decoder of claim 1, wherein each of the cascades of the second calculation unit contains a number INT(m/p) of processor elements, where p is an integer equal to or greater than 2 and less than m.

3.   (Original)   The Viterbi decoder of claim 2, wherein each of the INT(m/p) processor elements within a cascade are associated with one, and only one, of INT(m/p) successive disjunct p-bit groups of the m bits.

4.   (Original)   The Viterbi decoder of claim 2, wherein the numbers m and p are such that m/p is an integer.

5.   (Original)   The Viterbi decoder of claim 2, wherein the numbers m and p are such that m/p is not an integer and in addition to the INT(m/p) processor elements, each cascade further comprises an additional processor element associated with that an r-bit group which is formed as the remainder after removal of the INT(m/p) p-bit groups.

6.   (Original)   The Viterbi decoder as claimed in claim 5, wherein the additional processor element is associated with the r most significant bits or with the r least significant bits of the m bits.

7.   (Original)   The Viterbi decoder of claim 1, wherein each processor element comprises an addition device for generating a sum of two numbers, one of which is represented as a binary number by an associated group of branch metrics bits and the other of which is a redundant representation of the associated group of the bits of a previously selected path metric.

8.   (Original)   The Viterbi decoder of claim 7, wherein each processor element further comprises a modification device which receives as input variables the p least significant bits of said sum, the carry bit from the addition device of the processor element next in the cascade, a preliminary decision bit and a final decision bit from the processor element preceding it in the cascade, in order to produce a redundant representation of the associated group of bits in a preliminary path metric and a redundant representation of the associated group of bits in a final path metric.

9.   (Original)   The Viterbi decoder of claim 8, wherein each processor element further comprises a comparison device for forming the preliminary decision bit and the final decision bit for the subsequent processor element by linking the final path metric representation from the relevant processor element with the 2^X-1 preliminary path metric representations from other processor elements of the same order.

10.   (Original)   The Viterbi decoder of claim 8, wherein:
a first latch register is provided between the outputs of the addition device and the inputs of the modification device;
a second latch register is provided at the outputs of the modification device; and
the two latch registers are clocked with an offset of half a period of a clock rate.

[[10]]11.   (Currently Amended)   The Viterbi decoder of claim 8, wherein:
the redundant representations are thermometer representations, each comprising a u-bit word, where u is the most significant of the natural number to be

the redundant representations are thermometer representations, each comprising a u-bit word, where u is the most significant of the natural number to be represented, and the actual value v is represented by a same preselected binary value for all, and only all, of the v first bits; and

the selection device contains a number u of logical OR gates, each of which receives the 2^x bits of the same order from the thermometer representations of those preliminary path metric bits which are associated with the relevant group of branch metric bits, so that each of said OR gates produces at its output one of the u bits in the thermometer representation of the associated bit group in the previously accumulated extreme path metric.

[[11]]12.   (Currently Amended)   The Viterbi decoder of claim [[10]]11, wherein p = 2 and u = 4.

[[12]]13.   (Currently Amended)   A Viterbi decoder for decoding a convolutional code on the basis of a Radix-2^x trellis with 2^z states, where x and z are integers ≥ 1, comprising:

a first calculation unit which uses periodically successive multibit words in an input sequence for each trellis state to calculate the 2^x branch metrics as multibit words; and

a second calculation unit which, for each trellis state in each clock period, adds the respectively associated 2^x branch metrics to the already accumulated 2^x path metrics from 2^x predecessor trellis states and selects those of the 2^x path metrics which have been determined in a preselected sense to be as extreme as the new accumulated path metric for the addition process in the next period, wherein the second calculation unit contains, for each trellis state: a number 2^x of parallel cascades of processor elements which are connected in series for pipeline processing of the bits in the branch metrics and in the extreme path metrics, progressively with decreasing significance value of the bits, and in each case one extreme value selection device for all the processor elements of the same order within the pipeline, and the number of processor elements in each of the cascades is less than the number m of bits which are used for the binary number representation of the value range of the path metrics.

[[13]]14.   (Currently Amended)   The Viterbi decoder of claim [[12]]13, wherein each of the cascades of the second calculation unit contains one number INT(m/p) of processor elements which corresponds to the integer number of m/p, where p is an integer that is at least equal to 2 and is less than m, and where each of these INT(m/p) processor elements within the cascade is associated with one, and only one, of INT(m/p) successive disjunct p-bit groups of the m bits.

[[14]]15.   (Currently Amended)   The Viterbi decoder of claim [[13]]14, wherein the numbers m and p have magnitudes such that m/p is an integer.

[[15]]16.   (Currently Amended)   The Viterbi decoder of claim [[13]]14, wherein m/p is not an integer, and wherein, in addition to the INT(m/p) processor elements, each cascade contains an additional processor element which is associated with an r-bit group which is formed as the remainder after removal of the INT(m/p) p-bit groups.

[[16]]17.   (Currently Amended)   The Viterbi decoder of claim [[15]]16, wherein the further processor element is associated with the r most significant bits or with the r least significant bits of the m bits.

[[17]]18.   (Currently Amended)   The Viterbi decoder of one of claims claim [[12]]13, wherein each processor element comprises:

an addition device for formation of the sum of two numbers, which is represented as a binary number, one of which is represented as a binary number by the associated group of branch metrics bits and the other of which is a redundant representation of the associated group of the bits of the previously accumulated extreme path metric;

a modification device which receives as input variables the p least significant bits of said sum and the carry bit from the addition device of the processor element which is next in the cascade, as well as a preliminary and a final decision bit from the processor element which precedes it in the cascade, in order to produce a redundant representation of the associated group of bits in a preliminary path metric and a redundant representation of the associated group of bits in a final path metric; and

a comparison device which, by linking the final path metric representation from the relevant processor element with the 2^x-1 preliminary path metric representations

from the other processor elements of the same order, forms the preliminary decision bit and the final decision bit for the subsequent processor element.

[[18]]19.   (Currently Amended)   The Viterbi decoder of claim [[17]]18, further comprising:

a first latch register between the outputs of the addition device and the inputs of the modification device; and

a second latch register at the outputs of the modification device, wherein the two latch registers are clocked with an offset of half the period of the clock rate.

[[19]]20.   (Currently Amended)   The Viterbi decoder of one of claims claim [[17]]18, wherein:

the redundant representations are thermometer representations, each comprising a u-bit word, where u is the most significant of the natural number to be represented, and the actual value v is represented by a same preselected binary value for all, and only all, of the v first bits, counting from a preselected end of the word; and

each extreme value selection device contains a number u of logical OR gates, each of which receives the 2^x bits of the same order from the thermometer representations of those preliminary path metric bits which are associated with the relevant group of branch metric bits, so that each of said OR gates produces at its output one of the u bits in the thermometer representation of the associated bit group in the previously accumulated extreme path metric.

[[20]]21.   (Currently Amended)   The Viterbi decoder of claim [[12]]13, wherein the extreme path metrics are the respective maximum path metrics.